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1998 Technology Roadmap For Integrated Circuits Used in Critical Applications

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Abstract

Integrated Circuits (ICs) are being extensively used in commercial and government applications that have extreme consequences of failure. The rapid evolution of the commercial microelectronics industry presents serious technical and supplier challenges to this niche critical IC marketplace. This Roadmap was developed in conjunction with the Using ICs in Critical Applications Workshop which was held in Albuquerque, NM, November 11-12, 1997.

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1. EXECUTIVE OVERVIEW

At one end of the spectrum of uses of integrated circuits (ICs) are the applications with extreme consequences of failure. We call these “critical applications.” Failure of ICs in these applications can result in personal injury or loss of life, huge financial losses, compromised national security and other very undesirable effects. Some representative examples include medical electronics, electronic commerce, transportation, space and defense systems.

The use of ICs in critical applications presents serious technical and supplier challenges. Confidently assuring a given level of reliability, especially in a timely and affordable manner, is difficult. The typically small volume of ICs used coupled with concern about liability issues has made the mainstream IC suppliers reluctant to support this market segment. These technical and supplier challenges become especially acute when the critical application needs to use the IC outside of the commercial manufacturers specified lifetimes or environments (as often occurs, especially in space and defense applications).

Furthermore, the challenge of critical applications will grow considerably in the next decade as a result of profound changes in the IC industry. As scaling of ICs approaches fundamental limits, manufacturers are being forced into making major changes in the way ICs are made. This will result in less robust ICs and increases the risk of higher failure rates and new failure modes. The escalating costs of IC fabs will make critical applications an even less attractive market niche.

The ability to confidently, affordably and rapidly realize the benefits of advanced microelectronics in critical applications is a serious issue for individual organizations and for the country as a whole. The outlook is not promising under the status quo.

Proactive programs need to be established if we are to meet the challenge of using ICs in critical applications. To begin developing a strategic plan and a strategic partnership a Workshop on Using ICs in Critical Applications was held in Albuquerque, New Mexico in November, 1997. The purpose of the workshop was to bring together diverse members of the critical IC community to review current approaches and to identify future needs. Copies of many of these presentations can be viewed that the website at http://www.sandia.gov/eqrc/critical.

A second purpose of the Workshop was to develop a first version of a technical Roadmap. This document is the output of that process. The goal of this first version of the Roadmap was to document the major consensus technical trends impacting critical ICs and the major technical needs. Timelines for developing solutions will be added in the second edition of the Roadmap, which will be developed in conjunction with the Second Workshop which is scheduled to be held in Albuquerque at the beginning of May 1999.

The Critical IC Community has two major needs: supplier management and the development of new technologies.

The major supplier management issues are:

- The decreasing number of suppliers focused on critical ICs
- The inability to get needed information about commercial IC companies
- The rapid evolution of the commercial technologies
- The challenge of running captive fabrication facilities aimed at niche markets

The major technical needs are:

- The development of predictive reliability models
- The development of powerful yet practical reliability engineering tools
- The applicability of the tools and models to nonstandard environments
- The development of effective small lot qualification procedures
- The ability to screen out problem parts

New strategies will be required to effectively, confidently and affordably use ICs in critical applications. Separate strategies will be need for COTS ICs and custom ICs from captive fabs. One thing that will be required is greater interaction and cooperation among the diverse members of the critical IC community.

Solution of the supplier issues and development of the needed technical capabilities is often beyond the resources of the organizations involved in niche critical IC applications. A national focus on these problems is required. Many of the critical applications involve government programs and it is the public at large that is most at risk from failures of critical ICs.

Establishing the technology base to enable confidently and affordably realizing the benefits of advanced electronics technologies in high consequence of failure applications should be a high priority of national technology development programs. The Using ICs in Critical Applications Workshop and Roadmap can be an effective focal point for organizing these new national initiatives.

2. INTRODUCTION

Integrated Circuits (ICs) are finding extensive use in products and systems that have extremely high consequences of failure. Example applications include defense systems, medical electronics, communications, transportation, satellites, and electronic commerce. Failures of ICs in these applications can result in loss of life, threaten the public safety, imperil the national defense, and/or cause significant financial loss.

The decade ahead will be both an exciting and challenging time for the critical IC community. Future ICs will offer incredible advances in functionality and performance. They will also be less robust (e.g., with smaller voltage tolerances) and will entail a higher risk (e.g., they will incorporate clusters of not fully characterized new materials such as Cu interconnect/low K dielectrics or alternated gate insulators). This may be an especially challenging time for users who require extra reliability (or extra confidence in reliability) and/or non-benign environments and/or long lifetimes. The Sematech Reliability Roadmap reported that since 1994, reliability levels are no longer continuously improving and that there is a real risk of degradation of reliability in the rapid, discontinuous evolution of the IC industry.

The challenges facing mainstream digital CMOS technology are daunting enough. Specialty technologies, such as mixed analog/digital, nonvolatile memory, and IMEMS (Integrated Micro Electro Mechanical) have all of the challenges of digital technologies plus additional challenges specific to their technology. These technologies are essential for key critical applications of integrated circuits.

In addition to the technical challenges, there are supplier-side challenges. At one end of the supplier spectrum are COTS (Commercial-Off-the-Shelf) parts for which the specifications and/or level of information provided are not sufficient to support high confidence in critical applications. At the other end of the supplier spectrum, the low volume captive fabs (microelectronics manufacturing lines) face growing technical and economic challenges as they need to stay within 2-3 generations of the leading edge commercial fabs.

The technical and economic strategies currently used in the critical IC community will need to be reexamined in light of the profound changes in microelectronics technology.

The current state of the knowledge base, engineering tools, and supplier base present a serious challenge to the ability to fully utilize the benefits of advanced microelectronics technology in critical applications. Under the status quo, the future challenges will be even greater.

2.1 Purpose of Roadmap

The overarching motivation for developing the National Technology Roadmap for Integrated Circuits Used in Critical Applications (Critical IC Roadmap) is to stimulate the timely and effective development of the infrastructure required to be successful in using ICs in high consequence of failure applications.

The role of the Critical IC Roadmap in achieving this goal is to develop and document a consensus view of the technical capabilities required to successfully use ICs in critical applications. The Roadmap should provide guidance for the public and provide sponsors of R&D who are concerned with ICs used in critical applications. It will also provide guidance to university, industry and government R&D groups working on solving these challenging technical problems.

2.2 Scope of Roadmap

There is a lot of ground to be covered in fully describing the broad spectrum of issues facing the critical microelectronics community. To make it tractable to generate this first edition of the Roadmap, the scope has been focused on the most important, most crosscutting, widest impact issues. Subsequent editions of the Roadmap, as well as other publications, will consider a broader range of topics.

This first edition of the Roadmap focuses primarily on the technical issues associated with digital CMOS ICs since they constitute the majority of integrated circuits produced. Furthermore, many of the concerns and required technologies for digital CMOS will apply to other microelectronic technologies as well.

This first edition also presents a generic overview of some of the important supplier issues that need to be addressed.

2.3 Relationship to SIA National Technology Roadmap for Semiconductors

The Critical IC Roadmap is meant to complement the Semiconductor Industry Association's (SIA) National Technology Roadmap for Semiconductor (NTRS). ***There is no official linkage this Roadmap and the NTRS, nor is there any official endorsement of this Roadmap by the SIA.*** The 1997 edition of the NTRS can be found on the Sematech Web Site at www.sematech.org.

The focus of the NTRS is on the technical challenges facing the mainstream commercial industry as it tries to maintain its historic exponential improvement in cost/performance (Moore's Law). The NTRS is the main reference used in this Roadmap to identify future trends in semiconductor technology.

The NTRS, by itself, does not adequately address the issues that are important to the critical IC community. It does identify some of the issues that are important to the critical IC community, but does not develop these issues in sufficient depth. Furthermore, many of the concerns of the niche critical IC marketplace are absent from the NTRS, as they do not make the "top ten" lists that are a feature of the 1997 NTRS.

Nor will the NTRS stimulate the R&D investment required to meet the needs of critical IC users. As the NTRS points out, there is a shortfall of hundreds of millions of dollars per year in R&D to meet the problems identified by the NTRS.

There are a number of other roadmaps, white papers, etc. that this Critical IC Roadmap will stay linked to. One example is the Reliability and Failure Analysis Roadmaps generated by Sematech.

2.4 Process for Developing the Roadmap

The process for developing the Roadmap was centered on the Using Critical Integrated Circuits in Critical Applications Workshop held 11-12 November 1997 in Albuquerque, NM. Prior to the Workshop, a representative group of critical IC stakeholders developed a preliminary outline of the issues. This outline was presented at the Workshop and the attendees had the opportunity to make suggested revisions. After the workshop, the suggested revisions were incorporated into a full version of the Roadmap, which was then posted on the Web for additional comments. The final version was distributed in August 1998 to all Workshop attendees. In the following months, presentations on the Roadmap will be made to organizations that sponsor R&D.

The Critical IC Roadmap activity is being sponsored and funded by the Electronics Quality/Reliability Center at Sandia National Laboratories as part of its mission to support critical electronics for the nuclear weapons of the Department of Energy's Defense Programs. The CALCE program at the University of Maryland, the Jet Propulsion Laboratory and the National Institute of Standards and Technologies are cosponsors.

2.5 Future Versions of the Roadmap

The rapid and profound changes in integrated circuit technologies require that this roadmap be periodically updated. As mentioned above the main source of information on these changes is the SIA's NTRS. It seems appropriate, therefore, that updates of the Critical IC Roadmap be synchronized with the NTRS. At present, we plan to publish an updated Critical IC Roadmap approximately 6 months after the publication of each new NTRS. The NTRS is now planned to be issued every two years, with the next version due at the end of 1999. Therefore, the next Critical IC roadmap will be issued around the spring of 2000.

2.6 Roadmap Web Site and Contacts

The Roadmap and related information will be available through the homepage of Sandia National Laboratories' Electronics Quality/Reliability Center (EQRC) at

www.sandia.gov/eqrc

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3. CRITICAL VS. NON-CRITICAL APPLICATIONS

All other things being equal, virtually every user of ICs wants the highest reliability possible, as well as the highest performance, quickest time to market, and lowest cost. However, tradeoffs must be made between cost, performance, time to market, reliability and other customer requirements. In designing, manufacturing and testing ICs the manufacturers make technical and economic choices and tradeoffs that lead to a best combination of cost, performance, time to market and reliability for the market segment(s) they have targeted.

What distinguishes the critical IC market is a relatively greater value placed on confidently ensuring that reliability requirements are met. Users would prefer not to pay any penalty for this extra reliability assurance. In practice, some critical application users are willing to accept a reasonable cost, performance and/or time to market penalty. The increased costs come from additional testing and screening. Some users use older generation ICs on the theory that with time the bugs with the new technology have been identified and worked out. This translates into a performance and functionality penalty, as well as issues with obsolete parts. Still other users maintain captive fabrication lines. This can involve a significant cost penalty (vs. a comparable high-volume mainstream commercial product), but allows the product and process to be optimized for the application. It also avoids any problems that could result when third party manufacturers make unpublicized changes to their manufacturing process, testing, etc.

This section introduces some of the generic, cross cutting characteristics of the critical IC community.

3.1 Low Volume Complex Electronic Systems

Critical applications typically require low volume, complex products. The complexity of the products makes analysis and reliability prediction difficult.

The low volumes of ICs used has several implications. First, this is not an attractive market segment for high volume mainstream IC manufacturers to focus on. Second, a fixed number of parts are required to demonstrate a given level of reliability. When only a small volume of parts are ultimately used in the real application, the overhead of conducting a large number of tests to demonstrate reliability can be prohibitive. Third, running a captive fab at low volumes provides a challenge for process control, defect reduction, etc. It is very difficult to optimize processes, obtain high quality and high yields without running high volumes of standardized products.

3.2 Required Reliability Levels

There are three reliability requirements:

Requirement	Units	Description
Initial quality	ppm	Fails incoming inspection
Early failures (infant mortality)	ppm	Failure during the first year
Long term reliability	fits	Failure after first year

(A fit is the one failure in 10^9 hours of operation).

A quantitative estimate of the reliability is often required in critical applications.

The reliability of the IC is only one element in the reliability of the critical system. There are reliability issues associated with other hardware elements (e.g., circuit boards) and with software. There can also be system level solutions to compensate for uncertain component reliability (e.g., redundancy).

3.3 Confidence in Reliability

The high consequence of failure of critical ICs drives a desire to have more assurance that the required levels of reliability have been achieved. Some critical IC users will, within reason, spend more on testing, screening and root cause analysis to improve confidence. However, in other critical applications, market pressures make it uneconomical to use screening.

There are several aspects to confidence. One is the familiar issue of confidence in statistical sampling. For the different statistical forms (e.g., normal, Weibull) that are used to describe distributions of failures, one can calculate confidence limits based on the sample size and degree of extrapolation. There also is the issue of confidence in the physical models and model parameters used in the reliability analysis.

Again, a quantitative estimate of the confidence is often required.

3.4 Liability Issues

Commercial developers and users of critical ICs face potentially large financial judgments if their product fails. Companies must be able to document that they did as much as was possible to ensure the reliability of their products.

The potential for liability exposure inhibits semiconductor manufacturers from working with critical users of integrated circuits. This is especially true when the parts are used outside of the specifications. The following quotations that appeared in the Nov. 1997 issue of Military and Aerospace Electronics (page 1) illustrate this point:

"We [Analog Devices] don't accept liability due to the abuse of these parts."

"…use of National parts outside the published data sheet limits voids all National Warranties"

"We [Texas Instruments Military Semiconductors] cannot be liable for misuse of a part"

Also, most IC manufacturers publish a disclaimer in their databooks that prohibits the use of their ICs in medical life support (pacemakers and the like) without explicit written consent of their CEO.

3.5 Nonstandard Environments/Extended lifetimes

Some critical IC applications involve environments and lifetimes comparable to those applicable to the mainstream IC users. However, for many critical IC market segments the environments and/or lifetimes required exceed commercial requirements. Nonstandard environments include extended operating temperature ranges, shock/vibration, and radiation. Lifetimes have been several decades longer than the typical 5 to 10-year commercial specifications. (Many high volume commercial products – e.g., PCs, VCRs, are used on the average for only a few years before being replaced.)

To use ICs in these applications, some means, such as testing and screening, needs to be employed to ensure that the parts can be used outside of the manufacturer's data sheet. There is the additional challenge of ensuring that the parts actually used in their systems are exactly the same as the those that were used to establish that sufficient excess margin existed. This is made difficult by the rapid, often undocumented, changes that IC manufacturers make in their products. Environmental requirements for specific applications are considered in the next chapter.

3.6 Dormant Continuous Operation

The operational characteristics of critical IC applications vary between two extremes. At one end of the spectrum are devices that are operated only infrequently or only once (e.g., weapons). At the other end of the spectrum are some critical applications that must operate 24 hours a day, 7 days a week, 365 days a year (e.g., financial transactions, life support, safety sensors).

3.7 Competitiveness

Manufacturers of critical ICs also need to focus on their competitiveness. All of the typical competitive pressures - cost, time to market, performance advantages, etc. - also apply to this market segment. Therefore, critical IC users want to achieve higher reliability and higher confidence without significant penalties in cost, performance or time to market.

Today, government programs face significant budget pressures. These programs also need to assure reliability and confidence at a reasonable cost and in a reasonable time.

4. THE CRITICAL APPLICATIONS COMMUNITY

There is a very diverse community of applications in which IC failures are critical. A feeling for the diversity of the marketplace can be found in the papers presented at the Workshop. PDF versions of the following papers are available on the World Wide Web at http://www.sandia.gov/eqrc/critical

Richard E. Anderson, SNL
Failure Analysis Challenges for Sub 0.25µM Technologies

Connie S. Beane, FAA
Use of Integrated Circuits in Commercial Aviation

Edward I. Cole, SNL
Transient Power Supply Voltage Analysis for Detecting Defects

Theodore A. Dellin, SNL
Critical Applications Community

Theodore A. Dellin, SNL
Economic & Silicon Trends in the Commercial Industry and Their Impact on ICs Used in Critical Applications

Theodore A. Dellin, SNL
Advanced Integrated Circuit Reliability, Failure Analysis & Test at SNL's EQRC

Paul V. Dressendorfer, SNL
Packaging Trends

Ron Kalin, Medtronic
Reliability of Life Support Medical Electronics

Loren W. Linholm, NIST
Overview of the Roadmap and Workshop

Brent T. Meyer, SNL
Integrated Circuits in Nuclear Weapon Applications

Gary Nelson, Boeing
Critical IC Issues from an Aerospace Perspective

Gerald E. Servais, Delco
Criteria For Critical Integrated Circuits

Jerry M. Soden, SNL
Testing Trends

5. THE IMPACT OF THE COMMERCIAL MICROELECTRONICS INDUSTRY ON THE CRITICAL APPLICATIONS COMMUNITY

The purpose of this section is to describe the issues affecting the IC industry that impact the critical IC community. Issues such as lithography, which, while important to the mainstream IC industry, are not especially important to the critical IC community.

5.1 Sources of Information About the Commercial Industry

5.1.1 SIA Roadmap

The Semiconductor Industry Association (SIA) publishes the National Technology Roadmap for Semiconductors (NTRS). The NTRS is the main reference for the information presented in this section. The 1997 edition is widely available.

The SIA Roadmap is focused on identifying the top 10 difficult challenges in each of the 11 areas. The areas most important to the CAC are: Design and Test; Modeling and Simulation; Assembly and Packaging; Process Integration, Devices and Structures (most of the reliability issues are treated in this section); and Defect Reduction. Appendix A lists the NTRS' major challenges in reliability, failure analysis and test.

The SIA Roadmap focuses on two time periods: present day (0.25 micron) to 2005 (0.10 micron); and 2005 to 2012 (0.05 micron). The Critical IC Roadmap will focus on the near term, present to 2005 time frame.

5.1.2 Sematech Quality and Reliability Roadmap

The Reliability Technical Advisory Board (1997) developed a roadmap during 1996 on major reliability challenges. The Roadmap is in final review at Sematech and should be available for general distribution in the near future.

5.1.3 Sematech Product Analysis Forum Failure Analysis Roadmap

The Proceedings of the 21st International Symposium for Testing and Failure Analysis (ISTFA '95) contains a description of this roadmap (page 1).

5.2 Economic Trends

5.2.1 Moore's Law

The semiconductor manufacturing industry has enjoyed an average compound annual growth rate of 15% per year and is committed to staying on this growth path. This means that the industry needs to focus on finding major new customers and historic customers

with high turn over rates (e.g., personal computers that have a 2-4 year practical lifetime). The technology and product choices will be driven by this "sweet spot" in the marketplace. All niche markets, including critical ICs, will be increasingly constrained by the whims of the mainstream markets.

Historically the industry has realized this market growth by achieving 25-30% per year improvement in the cost per bit. This has been done through shrinking dimensions, increasing wafer sizes, improving yields and other improvements (such as equipment productivity). However, the yield and other improvements have reached a point where they are no longer able to make their historic contribution to staying on Moore's Law. The industry has compensated for this by being more aggressive in scaling. The rate of introduction of new technology nodes (e.g., going from 0.35 to 0.25 micron feature sizes) has been reduced from about every three years to two years or less.

The critical IC community will have to deal with a greater rate of change. One strategy previously employed is to stay one-to-two generations behind the leading-edge technology. The rationale behind this approach is that this will allow time to identify and resolve any problems with the new semiconductor manufacturing technology before its products are used in critical applications. If the rate of adoption of new technology generations is accelerated, the critical IC community will have less "breathing room" before being forced to adopt new technologies.

5.2.2 Economic Trends

There is a second Moore's Law: the cost of a new semiconductor manufacturing plant doubles with each new technology generation. One significant factor is that economics dictates that with each new generation the minimum number of wafer starts per month increases. Factories today have a capacity of 20,000 wafer starts per month and this is projected to grow to 30,000 to 40,000 starts in the next decade. The switch in the near future from 8" to 12" wafers will approximately double the number of die/wafer. Thus the number of die started per month will go up even more dramatically. Finally, the value per wafer will increase as dramatically. (A 12" wafer containing high end products could have a potential revenue of over $50,000.) As a result, the focus on improving yields will be even more intense.

For this and other reasons, the industry will be focusing on very large volume users and on developing standardized products with wide appeal. It also means that maintaining a captive fab to serve a niche market will become increasingly expensive.

5.2.3 Liability Concerns

There is some anecdotal evidence that semiconductor manufacturers are reluctant to work with users of ICs in critical applications because of the potential for being liable if there should be a failure in those ICs.

5.2.4 Focus on High Turnover Markets

To maintain a 15% annual growth rate in the IC marketplace, requires high volume users. The market looks for new high volume users. Critical applications of ICs can offer this new type of marketplace (e.g., intelligent highways with sensor chips built into the roadway).

Another possibility is to focus on markets where there is a high turnover of ICs. Personal computers are an excellent example of this type of market where many users buy a new computer every several years. Up to now, IC manufacturers typically qualify their parts for less than 1% failures over a ten year life at a moderately elevated temperatures. It was felt that qualifying for this longer time provided some extra margin, especially when utilizing leading-edge products in new technology generations that were not fully stabilized.

However, the strongest pressure in this market place is for rapid introduction of high performing parts. Reliability can be traded off for higher performance. There is some anecdotal evidence that designers are pressuring reliability groups for relief from reliability design rules when there is a clear performance advantage. This could take the form of a qualifying mainstream parts for 5 instead of 10 years. This would be of specific concern to users with long life critical applications. It would also be a generic concern to critical IC users because the parts would in general be less robust.

5.3 Design Trends

The design complexity (number of transistors per chip) is increasing at 58% compound growth rate, outstripping the 21%/year growth in designer productivity. The issue is not just the growth in the number of transistors, but also the need to use smaller transistors. Smaller devices have less drive strength and are more noise sensitive.

Testability is not explicitly incorporated into most designs. The use of scan techniques is becoming common in some types of products. The use of BIST (Built In Self Test) is infrequent.

Verification and analysis are serious bottlenecks for the timely design of systems and ICs. Verification can take up to one half of the total design process time.

High speed ICs dissipate proportionately increased power. This requires strict attention be paid to junction temperature, thermal design and thermal management/cooling techniques.

5.3.1 Design Complexity

The complexity of designs (number of transistors per chip) is growing exponentially at 58% per year. Designer productivity is increasing at about half this rate which leads to an increase in the size of design teams. A major reason for the slower productivity growth rate is that the capabilities of the ad hoc, loosely coupled collection of design tools and techniques is not keeping pace with the rapid advances in technology and design complexity.

5.3.2 Design for X

5.3.2.1 Design for Reliability

Design for reliability is accomplished through the use of design rules, which are aimed at preventing end-of-life failures from common failure modes such as dielectric breakdown, hot carrier degradation and electromigration. There are several simulators available that can analyze time dependent reliability effects on small circuits.

5.3.2.2 Design for Test and Verification

Design for Test and Design for Verification is not explicitly incorporated into most designs.

5.3.2.3 Design for Failure Analysis

Design to make failure analysis easier is not widely practiced.

5.3.3 BIST

Built-in self test techniques are not typically used, except in memory products.

5.4 Silicon Technology Trends

5.4.1 Scaling

Geometric dimensions and supply voltages are being scaled down with each new technology node.

Subthreshold leakage does not scale leading to an increase in background currents. This increase in background currents may make Iddq testing less effective.

5.4.2 Loss of Margin

Voltage threshold margins will stay about 10% of the supply voltage. Thus, as the supply voltage decreases, the absolute value of operating margin will also decrease. At

low supply voltages, noise and voltage overshoots become much greater issues to deal with.

5.4.3 Introduction of New Materials

The Integrated Circuit industry has historically been very conservative about the introduction of new materials into processing. At its most aggressive, it would introduce one new material per technology generation. However, with the ever increasing processing and device physics challenges of each new generation, the industry must introduce multiple new materials per generation. Furthermore, these new materials will not have the level of characterization (particularly for reliability issues) that have been required for past material introductions. The result will be a significant risk of new reliability problems (problems at the edges of distributions, new failure modes, unknown processing variables that affect reliability). This is especially true if the critical IC is used for extended times or in harsh environments

Two major, imminent, material substitutions will be the Cu interconnect and low K (low dielectric constant) interlevel dielectrics. The goal is to overcome the RC delay time associated with the interconnect. As devices are scaled down, the interconnect time constants become a more important factor in overall device speed. In laboratory experiments Cu has been shown to have better electromigration and stress voiding characteristics than Al interconnect. This has to be verified in full scale, high volume manufacturing. Cu is a highly diffusive species and if it gets into junctions, it can increase junction leakage. Barrier layers are required to keep the Cu from diffusing. Again, it remains to be seen how well this works in practice. Low K materials are being introduced to reduce capacitance and cross talk between adjacent metal lines. The issues with low K dielectrics are their thermal properties and long term stability. Critical applications that involve high temperatures and/or long lifetimes will be the most sensitive to the transition to Cu and low K.

5.5 Packaging Trends

There will be more interaction between the die and the package, particularly in the area of thermal management, noise management and mechanical stresses. Tighter coupling between the design of the die, the package and the Printed Circuit Board will be required.

5.5.1 Plastic packages

Plastic packaging has almost totally replaced ceramic packaging in high volume mainstream ICs. Similarly, in critical applications, the use of ceramic packages is diminishing.

5.5.2 Flip Chip

Stresses between the substrate and the die due to differences in the thermal coefficients of expansion requires the use of underfill or other solutions.

The inability to "see" the front surface of the packaged die requires the development of failure analysis techniques that can be provided from the backside of the die.

5.5.3 Ball Grid Array

BGAs are gaining increase use for High I/O applications. They offer reduce R, L and C, smaller size, lower weight and higher manufacturing assembly yield.

5.5.4 Chip Scale Packaging

Chip Scale Packages (CSP) are very small packages with about only 20% more area than the chip being packaged. Their use is very limited at present.

5.5.5 MultiChip Modules

Two issues with MCMs are the availability of known good die and the availability of known good substrates.

5.6 Testing Trends

Current approaches to testing are not meeting industry's speed and cost goals. Yet there is no clear alternative on the horizon to replace the current test paradigm.

5.6.1 Functional Testing

Functional verification of complex designs remains a challenge. Verification can take from a third to a half of the time required to develop a product.

5.6.2 Parametric Testing

The increase in the timing accuracy of testers (improving at 12%/year) is not keeping pace with the increase in chip speeds (increasing at 30%/year). At this rate tester errors will be greater than clock frequencies in a decade. As this point is approached, there will be increased yield losses resulting from increased guard bands in testing, or there will be a greater risk that parts will be shipped that do not fully meet their timing requirements

5.6.3 Defect Testing; IDDQ

Testing remains a critical way to identify manufacturing defects. This information prevents defective products from being shipped to customers and provides feedback to manufacturing (after failure analysis has been performed) to correct the source of those defects.

The increase in background currents with each new technology generation is reducing the ability of IDDQ testing to identify defective die.

5.7 Reliability Trends

The Sematech Reliability Technical Advisory Board has reported that reliability levels, which had previously monotonically improved with time, have been essentially flat since 1994. Furthermore, it is predicted that the levels will either remain flat over the next couple of years or might even get worse due to the rapid introduction of new materials that are inadequately characterized for reliability issues.

The major reliability issues addressed in the SIA Roadmap are the risk of introducing new, inadequately characterized materials into production and the need for design-for-reliability. Furthermore, there is a concern that the defect levels associated with the first products produced in new generations of technology are inconsistent with customer reliability requirements. (Rules of thumb used are that 1/100 to 1/500 of the yield fallout gives a good prediction of the number of early life failures.)

The major issues raised in the Sematech Reliability Roadmap are:

1. Silicon Technology Constraints
- 1.1. Reliability of gate dielectrics
- 1.2. Electromigration
- 1.3. Electrostatic discharge
- 1.4. Multilevel Metal/Dielectric Integrity
- 1.5. Hot Carrier Injection

2. Packaging Reliability
- 2.1. Integrity of organic interfaces after thermal, humidity or mechanical stress
- 2.2. Integrity of 1st level package interconnections (chip-to-package internal connections) after thermal, humidity, or mechanical stresses.
- 2.3. Integrity of 2nd. Level package interconnections (package-to-board connections) after thermal, humidity or mechanical stress.
- 2.4. Modeling for age, wearout and correlation to environmental stress

3. Design
- 3.1. Accuracy of design models
- 3.2. Design tools/metrology
- 3.3. Noise/crosstalk/latchup
- 3.4. Design for Testability
- 3.5. Low Iddq

4. Test, Diagnostics and Failure Analysis
- 4.1. Diagnosibility and Failure Analysis (essentially the Sematech FA Roadmap)
- 4.2. Test coverage and Known-Good-Die

4.3. Application vs. test program correlation
4.4. Self test
4.5. Iddq required

5.8 Failure Analysis

The Sematech Failure Analysis Roadmap calls for both evolutionary and revolutionary developments. Failure analysis tools must continuously improve to be able to deal with silicon technology trends such as smaller feature sizes, increased number of interconnect levels and higher operating frequencies. On the revolutionary side, there is a need for backside analysis techniques (to handle flip chip and dense, multilevel interconnections) and software based tools to allow rapid, low cost analysis.

6. SUPPLIER ISSUES

6.1 Commercial Off The Shelf (COTS)

Most integrated circuits used in critical applications are COTS (Commercial Off The Shelf) products. When these parts are used within the manufacturer's published specifications, the issue for the critical user is their level of confidence that the manufacturer's specifications have been met. Another issue is that critical applications are often sensitive to unspecified electrical parameters. The user needs to determine how they impact a given design. Furthermore, the critical user has to deal with the fact that the manufacturer may not be controlling these unspecified parameters.

6.1.1 Rapid Obsolescence of COTS and Sunset Technologies

There is a trend in the commercial industry toward more compressed product life cycles. This has resulted in an increase in end-of-life notices and product discontinuances for COTS ICs. The critical IC user has to plan for the contingency of a given part be no longer available.

The lifetime for a given manufacturing technology is also been compressed. Therefore, the time for a technology to become a "sunset technology" (i.e., a technology no longer available from mainstream suppliers) is being reduced. The critical IC user has to also plan for the contingency of the technology no longer being available. One strategy for this is the use of after market suppliers.

These obsolescence of parts and sunset technologies are motivations for establishing captive fabs.

Aftermarket suppliers (fabs) represent an alternative to obtaining both EOL parts and sunset technology parts but present some potential risks. Some of the issues that need to be addressed when considering the use of aftermarket suppliers are:

- Is the same fab, assembly and test equipment used to manufacture, assemble and test these ICs as the original source of supply?
- Some of the equipment used by the original manufacturing source is no longer available. Thus, new generations of equipment are used in conjunction with the older equipment. Have these processes and ICs been characterized for this mix-and-match combination of old and new equipment? * What is the yield? How does it compare with the original source of supply.
- Lack of high volume production lines does not allow fine tuning and debugging (optimization) of processes and yields.
- What is the adequacy of the test equipment? How does it compare with that used by the original source of supply? What is the adequacy of the test coverage. Who generated the test vectors?

6.2 Modified Commercial Off the Shelf (MOTS)

Some critical applications require use of products outside of the manufacturers published specifications. These parts are referred to as MOTS (modified off the shelf). In these cases, users try to ascertain that the parts have margins that allow use at higher temperatures, longer times, under irradiation, or under other conditions necessary for the critical application. This often involves extra testing and screening.

Using MOTS parts is challenge. The fact that one set of parts may be suitable for out-of-specification application does not ensure that other samples will. For example, commercial manufacturers of microelectronics often make documented (via Product Change Notice) and undocumented changes in their products (materials, dimensions and/or manufacturing processes). These changes could reduce or eliminate the excess margin that the critical user was depending on.

Commercial IC manufacturers generally do not cooperate with users who want to use their parts outside of published specifications. Indeed, they generally oppose those applications and warn that additional screening could cause unanticipated problems.

6.3 Specialized Fabs

In some critical applications specialized, often captive, fabs are used. These fabs are generally not at the leading edge of semiconductor technology. However, they eventually will have to track the trends presented in the NTRS. This results from the fact that these custom fabs must depend on the same equipment and supply as the commercial industry.

7. STRATEGIES FOR THE CRITICAL APPLICATIONS COMMUNITY

7.1 Extra Screening and Testing

The time and added cost associated with testing and screening is a major issue in mainstream applications. The CAC community generally does more testing than mainstream applications. At the wafer level Iddq testing as well as a high voltage stress test may be used to weed out defective parts.

7.2 Captive Fabs

Some developers of high consequence electronic products have captive IC fabrication facilities (fabs). One advantage is that captive fabs optimize the technology for the application.

7.3 Staying away From Bleeding-edge Technologies

Segments of the CAC industry, such as automotive, tend to avoid leading-edge technologies. By delaying adoption of a new technology node reduces the risk of reliability problems and it also reduces costs. The downside is the performance penalty relative to not using leading-edge products. Another issue is the short product life of COTS ICs. Thus waiting to use the technology (delayed by 1-2 generations) may render the product obsolete.

7.4 Cooperation Among Different Users

Users of integrated circuits in critical applications have several things in common. Since they use small quantities of parts, they do not attract the interest of most suppliers (e.g., suppliers are not inclined to support this market segment). The second problem is the need for extra test requirements to ensure reliable operation in their systems. In addition, different users often search for suppliers of similar parts and do similar qualifications.

This suggests a strategy of cooperation among different users. Users can pool their efforts to avoid redundancy in evaluation and qualifying parts. They may also be able to combine requirements and pool purchases to be a more attractive customer segment using means such as industry cooperatives.

7.4.1 Databases

One method for sharing information would be to establish centralized databases of part characteristics. Data fields could include:

- User Environment & Requirements
- Recommendations to Users

- Manufacturer Test Data
- Reliability, Safety Predictions
- Field Test Data
- IC Supplier Characterization Data

7.4.2 Centers of Excellence

Another way to collectively help a broad base of users is through Centers of Excellence. These Centers can provide technical services and technical tools to help critical users be successful.

In the past the Department of Defense Rome Labs provided such support through its publications of Mil Handbooks. However, DoD has discontinued support of the Handbooks.

There are a number of Centers that are active today. Two examples are the Center for Computer Aided Life Cycle Engineering (CALCE) at the University of Maryland and the Electronics Quality/Reliability Center (EQRC) at Sandia.

[Note to readers: If you are aware of additional centers please send that information to Ted Dellin at dellinta@sandia.gov.

In addition, there are a number of organizations, while not specialized Centers of Excellence, can provide support in niche areas to the critical applications community.

7.4.3 Education and Training

The Critical Application Community needs to continually upgrade its technical skills (use of design tools, advanced statistical techniques, reliability physics and understanding of failure mechanism, functional team skills, supplier relations skills) to keep pace with the evolution of the microelectronics industry and the evolving challenges of critical applications.

7.4.4 Conferences and Workshops

Conferences and Workshops are required to bring the Critical Applications Community together to share the latest technical results and to discuss best practices.

7.4.5 Developing the Technology Base

Critical users should work together to develop the technical base required to support critical applications (See Section 8). This can be accomplished by directly sponsoring R&D and by influencing national sponsors of R&D to invest in these needed technologies.

Since major R&D sponsors (e.g., DoD and DOE) are concerned with critical applications they should be receptive to reflecting the needs of this community in their R&D portfolio.

7.4.6 Establish New Consortia/Cooperatives

Finally, it may be possible that a new consortia representing the Critical Applications Community (or national committee or other formal vehicle) may help facilitate the cooperative measures described below. This new entity might also help make this community more influential with R&D sponsors.

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8. THE TECHNOLOGY BASE FOR IMPLEMENTING CRITICAL APPLICATIONS COMMUNITY'S STRATEGIES

The purpose of this section is to describe the technology base required for Critical Applications.

8.1 Design for X

Methodologies can be employed during design that can improve the reliability, diagnosibility and other attributes of the product. This is referred to as Design for X (DFX) where the X can stand for reliability, manufacturability, test, failure analysis or other attributes.

8.1.1 Design for Reliability

Ensuring that the design adheres to the design rules established for a technology is the key to preventing end of life wearout. If burn-in is required, then parts also need to be designed for elevated temperatures to ensure that dynamic burn-in is possible.

8.1.1.1 Identification of New Failure Modes

The first step in Design for Reliability is to ensure that all significant failure modes have been identified. As microelectronics technology changes, the potential for unexpected new failure modes grows. New material introductions (such as the imminent introduction of Cu metallization and lower dielectric constant interlevel dielectrics) will bring new failure mechanisms. This must be understood.

A major emerging challenge is to identify the failure modes of micromechanical (MEMs) devices.

Use of parts outside of manufacturers' specifications also raises the risk of discovering new failure modes.

8.1.1.2 Predictive Reliability Modeling/Physics of Failure

At the heart of Design for Reliability - indeed almost all approaches to reliability - are predictive models. Models need to be developed for each significant failure mode. Physical models are required to predict reliability as a function of design variables (e.g., dimensions, voltages), processing variables (materials used, process parameters) and end use conditions (e.g., lifetime, maximum temperature). Statistical models are required to determine the shape of the distributions of times to failure. These models need to account for the effects of deep submicron phenomena.

Many critical applications need the above models to work outside of the commercial operating regimes.

8.1.2 Design for Testability

8.1.2.1 Scan

8.1.2.2 Built in Self Test (BIST)

BIST needs to be made usable in short-design cycle environments by novice designers. Logic BIST methods must be developed that give fault coverage for hard-to-target failures, and for all fault types required.

8.1.2.3 State of the Health Monitoring

Critical Applications would be enhanced if ICs could be electrically interrogated to determine if they are functioning properly. This interrogation could be at power up or on demand. The IC would send back a signal indicating if it is functioning properly or not.

8.1.3 Design for Verification and Failure Analysis

ICs need to have their physical layout and electrical design optimized to for rapid location of failure sites.

8.1.4 Design for Environment/Application

The ability needs to be developed to design ICs for the environmental stresses required by an application. There also needs to be system design tools that can be used to design the ability of the system to mitigate the effects of external environments.

8.2 Testing techniques

8.2.1 Functional and Parametric Testing

ICs are subjected by manufactures to testing at the end of fabrication, after packaging, and (if performed) after burn-in. There are two aspects to the testing. Functional testing provides a check that the device is performing the intended operations. Parametric testing is aimed at measuring operating characteristics.

8.2.2 Defect Testing; Iddq

Iddq testing is a powerful method for detecting existing and latent defects in integrated circuits. Iddq testing can be enhanced by designing circuits with low current states that permit the testing.

As ICs are scaled down the standby currents increase. These large leakage currents reduce the ability to detect defects with Iddq. An Iddq-like test needs to be developed for devices with high standby currents.

Standards are required for fault models and coverage metrics for these models, so that a common language can be used to describe fault coverage. Methods to test for new fault types must be developed

8.2.3. Calibration

It is important that all test equipment used with critical ICs be calibrated with standards that are traceable to National Institute of Science and Technology.

It is also important to understand the accuracy, repeatability and reproducibility of the data being measured and place quantitative error bars on reliability predictions.

8.2.4 Standardized Approaches

Standardized approaches are required for reliability characterization. This includes common test structures, tests, test techniques and means of interpreting the test data. These approaches would make reliability characterization more efficient and would facilitate sharing of characterization data.

8.3 Packaging

The switch to new types of packaging (flip chip, chip scale) and the use of new packaging materials presents challenges for ensuring reliability in critical applications.

8.3.1 Plastic packaging

The use of plastic packages in high reliability applications is an ongoing area of research.

8.3.2 Flip Chip/CSP

Flip chip packaging does not allow access to the front side of the die which contains the active circuitry. One challenge that this presents is the need to develop backside failure analysis techniques.

8.3.3 Known Good Die

Known good die are required for multipchip module applications.

8.3.4. Testing

Very high accelerated reliability testing techniques need to be developed that can screen new materials/designs/technologies and that can be related to actual field reliability.

8.4 Screening

Electrical or other screening that could eliminate burn-in is needed.

8.4.1 Upspecing

Predictive models for failure modes need to be developed and validated for extreme environments and for long lifetimes.

Additional information is required from manufacturers to be able to assess and qualify products used outside of manufacturer's specifications. Furthermore, a method needs to be developed to when incoming products design/processing/testing & screening has changed in a way that will impact the ability of the ICs to be used outside of their specified environments.

8.5 Qualification

It is very inefficient to have separate user companies characterizing the same parts. A means of exchanging data is required. This would be facilitated by common qualification standards and by common definitions.

New qualification evaluation tools and processes will be required. On the horizon is the use of comprehensive simulation models to predict reliability, doing away with traditional reliability testing.

8.6 Failure Analysis

Develop software tools for Failure Analysis, Design Debug and Design Simulation that bridge (merge) the hardware CAD capability and the firmware capability.

8.7 Fail Safe ICs

ICs could be developed that would always fail into a known state(s) this would help in implementing safety and security at the system level.

8.8 Self Repairing ICs

ICs could bring in redundant elements if a problem were detected

8.9 Solutions at the System Level

There are modifications at the system level that can compensate for poor or uncertain reliability and/or the inability to operate over extended environmental conditions. However, these solutions generally extract a cost, performance, weight or volume penalty at the system level. System level tools are required to design these system level modifications and to do the tradeoffs between more robust ICs and system level modifications.

8.9.1 Redundancy

The development of intelligent redundancy: systems that could reconfigure themselves to avoid defective ICs

8.9.2 Managing Environmental Stresses

The system can be designed to provide a more benign environment for the ICs. For example, cooling can be provided to reduce temperature extremes.

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9. ROADMAP PARTICIPANTS

9.1 Disclaimer

This Roadmap represents a good faith effort to develop a *consensus* view of the issues facing the Critical IC Applications Community. There are, of course, variations in the views between individuals and between organizations. Thus, like any Roadmap developed by a group, it does not necessarily represent the precise view of any one individual or organization. The listing of names and organizations in the Roadmap in general, and this section in particular, does not imply endorsement of all the recommendations presented in this roadmap.

9.2 Acknowledgments

Development of this Roadmap would not have been possible without the contributions of the individuals and organizations who are mentioned below. Their support is deeply appreciated

9.2.1 Sandia National Laboratories 1997 High Consequence Engineering Symposium Series and Strategic Surety Programs.

Financial support for the Workshop was provided by the Sandia High Consequence Engineering Seminar Series. Additional support for the Workshop and the Roadmap was provided by Sandia's Strategic Surety Program, Laura Gilliom, Program Manager.

9.2.2 Sponsoring Organizations

Sponsoring organizations provide support for one or more of their staff to work on the Workshop organizing committee or on the Roadmap committees. The support of these organizations is gratefully acknowledged.

9.2.3 Committees

9.2.3.1 Workshop Steering Committee (in alphabetical order)

Ted Dellin	Sandia National Labs
Andy Kostic	IBM
Loren Linholm	NIST
Mike Pecht	University of Maryland/CALCE

9.2.3.2 Roadmap Steering Committee (in alphabetical order)

Ted Dellin	Sandia National Laboratories
Gene Hnatek	Compaq Computer Corp./Tandem Division
Andy Kostic	IBM

Loren LinholmNIST
Mike Pecht University of Maryland/CALCE

9.2.4 Participants at the Using Integrated Circuits in Critical Applications Workshop, Albuquerque, New Mexico.

See Appendix C.

9.2.5 Support Staff

Viola Madrid of the Reliability Technologies Department, 1203 was the major support person who organized the Workshop and oversaw the production of the Roadmap. Her contribution is deeply appreciated.

Other Sandians who provided support are Dominque Foley-Wilson, Patti Sanchez, and Lupe Raines.

APPENDIX A:
SELECTED TOP 10 CHALLENGES
FROM THE 1997 NATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

Table 7 Design & Test Difficult Challenges

Five Difficult Challenges≥100 nm/Before 2006	*Summary of Issues*
Signal integrity and IC reliability	Noise, interconnect, and reliability related issues.

Table 9 Testing Difficult Challenges

Five Difficult Challenges≥100 nm/Before 2006	*Summary of Issues*
BIST and DTF	Test equipment costs will rise toward $20M and wafer yields will fall toward zero unless there is increased use of DFT and BIST.
IDDQ testing	This testing may not be viable when IC's contain tens of millions of transistors; circuit partitioning and built-in current sensors should be studied.
Fault models	New fault models will be needed for advanced, multi-level metal ICs; the traditional stuck at model is becoming less effective.
DFT	New DFT techniques (SCAN and BIST have been the mainstay for over 20 years; breakthrough tools for control and observation are needed.)
Failure Analysis	3-D CAD and FA systems for isolation of defects in multilayer metal processes.

Table 13 Process Integration, Devices, & Structures Difficult Challenges

Five Difficult Challenges≥100 nm/Before 2006	*Summary of Issues*
Management of increasing reliability risks with rapid introduction of new technologies	A cluster of new materials is being aggressively introduced; these typically require 5-10 years of R & D. Higher current densities, scaling, and increased power are not supported by new reliability models, databases and diagnostic/failure analysis tools.
Design for manufacturability, reliability, performance (DFX)	Inadequate smart design tools that incorporate integration challenges in process control, proximity effects, reliability, performance, etc. Validated 2-D/3-D* TCAD simulators for process control, reliability, performance.

**2-D/3-D--2- and 3-dimensional*

Table 19 Front End Processes Difficult Challenges

Five Difficult Challenges≥100 nm/Before 2006	*Summary of Issues*
Gate dielectric scaling (including surface preparation)	Issues of scaling gate dielectric to below 2 nm are control of tunneling currents, boron out-diffusion and gate dielectric penetration, and charge-induced damage.

Table 31 Interconnect Difficult Challenges

Five Difficult Challenges≥100 nm/Before 2006	*Summary of Issues*
Chip reliability	New materials and architecture (copper, low K, Damascene create some chip reliability exposure. Detecting, testing modeling, and control of new failure mechanisms will be key.

Table 42 Assembly & Packaging Difficult Challenges

Five Difficult Challenges≥100 nm/Before 2006	*Summary of Issues*
Reliability limits of flip chip on organic substrates	Comprehensive parametric knowledge of packaging components (chip size, underfill, substrate, heat sink, UBM/bump**).

***UBM-under bump metallurgy*

Table 54 Defect Reduction Difficult Challenges

Five Difficult Challenges≥100 nm/Before 2006	*Summary of Issues*
Fault isolation	Circuit complexity grows exponentially and the ability to rapidly isolate failures on non-arrayed chips is needed.
Failure analysis of nonvisual defects.	Techniques are needed to enable sourcing of defects where no physical remnant is detected.

Table 60 Metrology Difficult Challenges

Five Difficult Challenges≥100 nm/Before 2006	*Summary of Issues*
Standard electrical test method for reliability of ultra-thin silicon dioxide and new gate dielectric materials.	The wearout mechanism for ultra-thin gate dielectrics is thought to be different from that observed for silicon dioxide at the thickness used in the 250 nm technology generation.

APPENDIX B: TECHNICAL PROGRAM OF THE 1997 USING ICS IN CRITICAL APPLICATIONS WORKSHOP

Sandia National Laboratories' 1997 High Consequence Engineering Series

CRITICAL

USING INTEGRATED CIRCUITS IN CRITICAL APPLICATIONS

Albuquerque Wyndham Airport Hotel
November 11-12, 1997

SPONSORING ORGANIZATIONS

Electronics Quality/Reliability Center, Sandia National Laboratories
National Institute of Standards and Technology
University of Maryland Computer Aided Life Cycle Engineering Center
Jet Propulsion Laboratories

WORKSHOP PROGRAM

Tuesday, November 11, 1997

7:00 AM	Registration
	Continental Breakfast
8:00	Welcome……………… Laura Gilliom, Program Manager, Strategic Surety, SNL
	Overview of Roadmap Development Process
8:05	Process……………………………………………………Loren Linholm, NIST
8:20	Critical Applications Community………………………….. Ted Dellin, SNL
	Future IC Trends From the Perspective of Critical IC Users
8:35	Industry & Silicon Trends…………………………………..Ted Dellin, SNL
9:35	Packaging Trends…………………………………..Paul Dressendorfer, SNL
10:05	Break
10:25	Testing Trends…………………………………….…..Jerry Soden, SNL
10:55	Failure Analysis Trends………………………………...Rich Anderson, SNL
11:45	Lunch
1:00PM	***How Different Sectors Handle Critical IC Issues***
1:05	Space Systems……………………………………..…..Sammy Kayali, JPL
1:30	Defense Systems…………………………………..Michael Pecht, CALCE Patrick McClusky, CALCE
1:55	Biotechnology…………………………………...…. Ron Kalin, Medtronic Dennis Scranton, Medtronic
2:20	Computers…………………………………………….....Andy Kostic, IBM
2:45	Automotive……………………………………………Gerald Servais, Delco

3:10	Break
3:30	Aerospace…………………………………………..….Gary Nelson, Boeing
3:55	Aviation Regulation…………………………………….Connie Beane, FAA
4:20	Nuclear Weapons…………………………………………Brent Meyer, SNL
4:55	Panel Discussion
5:30	***Evening Homework Assignment***
	Read PreRoadmap
	Put Brainstorming Ideas on Post-its
5:35	Session Ends
6:00	**No Host Cocktail Hour** Bandalier Room
7:00	Dinner…………………………………………………….…... Bandalier Room
	Ballooning in Albuquerque
	Ray E. Bair, Director, Electronic Components Center, SNL

Wednesday, November 12, 1997

7:00 AM	Continental Breakfast
8:00	***Participants Place Brainstorming Ideas on Boards***
8:00	Announcements
	Emerging Solutions
8:05	A Successor to Iddq?…………………………………....Ed Cole, et. al., SNL
8:30	Fault Injection-Based Simulation……..Jagdish Patel, et. al., Univ. of Illinois
8:55	Sandia FA, Rel. & Test……………..………..….…………..Ted Dellin, SNL
	Developing the Roadmap
9:20	Overview of Roadmap Brainstorming Process
9:35	Brainstorming
10:30	Break into Topic Groups
	Coalesce Brainstorming Ideas
	Prioritize Brainstorming Ideas
11:00	Summary Report of Each Group
11:30	Lunch
1:00PM	***Vote on Priority Issues***
2:00	***Outline of Next Steps: Finishing the Roadmap***
2:20	**Bus Departs for Tour of Sandia's EQRC:**
	IC Reliability and Benchmarking
	Micromachine Reliability
	Advanced Failure Analysis Techniques
	Failure Analysis Expert System
	Bus Returns Attendees to Hotel

APPENDIX C:
WORKSHOP ATTENDEES

Name	Organization
Anderson, Richard E.	Sandia National Laboratories
Antonescu, Christina	US Nuclear Regulatory Commission
Bair, Ray E.	Sandia National Laboratories
Baird II, Eugene W.	Hughes Technical Services Company
Barnes, Charles E.	Jet Propulsion Laboratory
Beane, Connie S	Federal Aviation Administration
Bonn, Russell H.	Sandia National Laboratories
Borrego, Joe H.	Sandia National Laboratories
Brooks, Peter J.	Harris Semiconductor
Browning, John S.	Sandia National Laboratories
Brunamonti, Victor G.	Naval Surfaces Warfare Center/Crane Division
Caldwell, Michele	Sandia National Laboratories
Char, Melvin K.	Boeing Commercial Airplane Group
Clark, Kevin P.	Jet Propulsion Laboratory
Cochran, Bryan C.	Boeing Helicopters
Cole, Edward I.	Sandia National Laboratories
Dellin, Theodore A.	Sandia National Laboratories
Dressendorfer, Paul V.	Sandia National Laboratories
Emerson, John A.	Sandia National Laboratories
Gaona Jr., John L	Sandia National Laboratories
Geery, Brian L	Sandia National Laboratories
Gelet, David J.	Sandia National Laboratories
Hamari, Wayne L.	Rantec Microwave & Electronics, Inc.
Hamm, Bob	Hughes Space & Communications Co.
Hart, Douglas M.	Lockheed Martin Aero & Naval Systems
Hawkins, Charles F.	University of New Mexico/SNL
Henderson, James T.	Sandia National Laboratories
Hnatek, Eugene R.	Tandem Computers Inc.
Hudson, James F.	Sandia National Laboratories
Jen, Hei-Ruey	AMP M/A-Com
Kalin, Ron	Medtronic, Inc./Product Assurance Department
Kayali, Sammy A.	Jet Propulsion Laboratory
Kennedy, John G.	Storage Technology Corp.
Kostic, Andrew D.	IBM
Linholm, Loren W.	US Department of Commerce/NIST
Liu, Cyrus Y.	Hughes Aircraft Company
Lundberg, Lars	Swedish Defence Materiel Administration
Lussier, Gene	Technical Electronic & Manufacturing Services
McCluskey, Patrick	University of Maryland/CALCE
Mendoza, Ben	Logic Devices Inc.

Meyer, Brent T.	Sandia National Laboratories
Monroe, David K.	Sandia National Laboratories
Monson, Mary A.	Sandia National Laboratories
Moor, Andrew F.	Johns Hopkins University/APL
Mowrey, Rick C.	Honeywell, Inc.
Nedi, Assefa	National Semiconductor
Nelson, Gary L.	Boeing Information, Space & Defense Systems
Opalka, James M.	Sandia National Laboratories
Ortiz, Keith	Sandia National Laboratories
Panzer, Gary W.	Hughes Aircraft
Pecht, Michael	University of Maryland/CALCE
Pettit, Richard B.	Sandia National Laboratories
Poelking, Monica L	DSCC-VAC
Ryan, Patrick W.	Rantec Microwave & Electronics, Inc.
Scranton, Dennis	Medtronic Micro Rel
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